A 5.26 Mflips programmable analogue fuzzy logic controller in a standard CMOS 2.4 /spl mu/ technology

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RESUMEN

A complete digitally - programmable analogue Fuzzy Logic Controller (FLC) is presented. The design of some new functional blocks and the improvement of others aim towards speed optimization with a reasonable accuracy, as it is needed in several analogue Signal Processing applications. A nine-rules, two-inputs and one-output prototype was fabricated and successfully tested using a standard CMOS 2.4 µ technology showing good agreement with the expected performances, namely: 5.26 Mflips (Mega fuzzy logic inferences per second) at the pin terminals (CL = 13 pF), 933 µW power consumption per rule (Vdd = 5 V) and 5 to 6 bits of precision. Since the circuit is intended for a subsystem embedded in an application chip (CL≤5 pF) over 8 Mflips may be expected.