A linearly tunable low-voltage CMOS transconductor with improved common-mode stability and its application to gm-C filters

RESUMEN

A linearly tunable low-voltage CMOS transconductor featuring a new adaptative-bias mechanism that considerably improves the stability of the processed-signal common-mode voltage over the tuning range critical for very-low voltage applications is introduced. It embeds a feedback loop that holds input devices on triode region while boosting the output resistance. Analysis of the integrator frequency response gives an insight into the location of secondary poles and zeros as function of design parameters. A third-order low-pass Cauer filter employing the proposed transconductor was designed and integrated on a 0.8-/jm n-well CMOS standard process. For a 1.8-V supply filter characterization revealed fp = 0.93 MHz fs = 1.82 MHz Amin = 44.08 dB and Amax = 0.64 dB at nominal tuning. Tuned by a dc voltage VTUNE> the filter bandwidth was linearly adjusted at a rate of 11.48 kHz/mV over nearly one frequency decade. A maximum 13-mV deviation on the common-mode voltage at the filter output was measured over the interval 25 mV < VTUNE < 200 mV. For Vout = 300 mVpp and VTUNE = 100 mV THD was -55.4 dB. Noise spectral density was 0.84 V/Hz1/2 @1 kHz and S/N = 41 dB @Vout = 300 mVpp and 1-MHz bandwidth. Idle power consumption was 1.73 mW @VTUNE = 100 mV. A tradeoff between dynamic range bandwidth power consumption and chip area has then been achieved.

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