



A linearly tunable low-voltage CMOS transconductor with improved common-mode stability and its application to gm-C filters

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RESUMEN

A linearly tunable low-voltage CMOS transconductor featuring a new adaptative-bias mechanism that considerably improves the stability of the processed-signal common-mode voltage over the tuning range critical for very-low voltage applications is introduced. It embeds a feedback loop that holds input devices on triode region while boosting the output resistance. Analysis of the integrator frequency response gives an insight into the location of secondary poles and zeros as function of design parameters. A third-order low-pass Cauer filter employing the proposed transconductor was designed and integrated on a 0.8- μm n-well CMOS standard process. For a 1.8-V supply filter characterization revealed $f_p = 0.93$ MHz $f_s = 1.82$ MHz $A_{\min} = 44.08$ dB and $A_{\max} = 0.64$ dB at nominal tuning. Tuned by a dc voltage V_{TUNE} the filter bandwidth was linearly adjusted at a rate of 11.48 kHz/mV over nearly one frequency decade. A maximum 13-mV deviation on the common-mode voltage at the filter output was measured over the interval $25 \text{ mV} < V_{\text{TUNE}} < 200 \text{ mV}$. For $V_{\text{out}} = 300 \text{ mVpp}$ and $V_{\text{TUNE}} = 100 \text{ mV}$ THD was -55.4 dB. Noise spectral density was $0.84 \text{ V/Hz}^{1/2}$ @1 kHz and $S/N = 41$ dB @ $V_{\text{out}} = 300 \text{ mVpp}$ and 1-MHz bandwidth. Idle power consumption was 1.73 mW @ $V_{\text{TUNE}} = 100 \text{ mV}$. A tradeoff between dynamic range bandwidth power consumption and chip area has then been achieved.

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