



A 9.6 kb/s CMOS FSK modem for data transmission through power lines

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RESUMEN

The design and test of a mixed-signal 9.6Kb/s FSK transmitterreceiver is presented. It is aimed for digital communications through the domiciliary power lines as needed by a networked electrical power management and measuring system wherein the circuit must be embedded. For the desired baud rate the bit carriers frequencies of 111KHz (logical 0) and 125KHz (logical 1) were found optimal. The receiver amplifies and demodulates the incoming bit stream following a frequency-domain discrimination strategy based on switched capacitor (SC) filtering. The transmitter, pure digital, generates the carriers tones and builds the outgoing bit stream based on a frequency division technique by means of digital counters driven by a 6 MHz master clock. This can be either externally or internally generated and, as a byproduct, it is also used to handle the switches of the SC filters in the receiver. The circuit was fabricated in a standard 1.6um CMOS technology. For a $\pm 2.5V$ rail-to-rail power supply the die area results in 5.76 mm² whereas the current consumption is kept below 12mA. The modem was successfully tested within its own working environment. Main advantages with respect to its previously implemented discrete version by the OEM[1] reside in the extremely reduced number of external components required and the needlessness of a-posteriori filter tuning.

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