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Research Article

Applying the Analog Configurability Test Approach in a Wireless Sensor Network Application

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This work addresses the application of the analog configurability test (ACT) approach for an embedded analog configurable circuit (EACC), composed of operational amplifiers and interconnection resources that are embedded in the MSP430xG461x microcontrollers family. This test strategy is particularly useful for in-field application requiring reliability, safe operation, or fault tolerance characteristics. Our test proposal consists of programming a reduced set of available configurations for the EACC and testing its functionality by measuring only a few key parameters. The processor executes an embedded test routine that sequentially programs selected configurations, sets the test stimulus, acquires data from the internal ADC, and performs required calculations. The test approach is experimentally evaluated using an embedded system-based real application board. Our experimental results show very good repeatability, with very low errors. These results show that the ACT proposed here is useful for testing the functionality of the circuit under test in a real application context by using a simple strategy at a very low cost.

1. Introduction

Testing analog circuits in increasingly complex, faster, and denser integrated systems is a significant challenge. The low observability and controllability of the internal nodes and the complex nature of the signals involved make that particular test solutions be generated for specific sections. Another difficulty lies in the fact that analog faults do not cause a simple state change in the logic values, as in the case of its digitals counterparts [1]. The embedded analog configurable circuits (EACCs) available in modern microcontrollers (μC) present additional testing-related problems. The usually high number of configurations able to be programmed (and consequently to be tested) and the strong interaction between the digital and analog blocks, conditioning the access to analog sections through a complex digital interface, represent typical examples of these difficulties.

In both functional [2, 3] and structural [4, 5] approaches, the test of analog circuits has been widely discussed. However, the test of EACCs has been comparatively less explored. The first efforts for applying well-known test techniques to field programmable analog arrays (FPAAs) are reported in [6–8]. The authors apply oscillation-based test (OBT) for testing the configurable blocks of the ispPAC10 device from lattice and propose a test response analyzer configured in the device, evaluating its fault detection ability through fault injection in the capacitors, switches, and input amplifiers. The transient response analysis method (TRAM) is applied for testing an ispPAC10 and another FPAA device from Anadigm in [9, 10]. A proposal for testing FPAA interconnections between blocks is presented in [11, 12], addressing a particular FPAA device from Anadigm. Finally, an application-oriented test strategy is presented in [13], but it requires the application of neural networks with high computational demands. Broadly, the implementation of all the above-mentioned methods is feasible when high hardware overhead is acceptable.

Recently, a new self-test approach for EACCs, named analog configurability test (ACT), has been proposed in [14].

The main goal of this strategy is to determine the EACC configurations that can be successfully programmed. This is achieved by programming a reduced set of available configurations and by measuring only a few key parameters. In this approach, the processor core executes an embedded test routine that sequentially programs different configurations, acquires data from an embedded analog-to-digital converter (ADC), and performs required calculations.

ACT is attractive for critical systems requiring a circuit reconfiguration under fault conditions. In this context, ACT could periodically establish the configurations of the EACC that can be effectively programmed by the processor core, before a reconfiguration procedure. This is useful when the application demands fault tolerance characteristics. By another way, ACT could be part of a broader software-based built-in self-test (SW-BIST) strategy. In SW-BIST, a microprocessor core functions as pattern generator and as response analyzer to test other components embedded in the system [15, 16]. Within this context, ACT could be also used as a low-cost self-test procedure for maintenance purposes.

In this work, we apply the ACT concept to an EACC composed of operational amplifiers (OAs) and interconnection resources that is present in the MSP430x461x μCs family from Texas Instruments. It should be noted that the EACC addressed here has different structure and functionalities than the used in [14]. Additionally, the resources available on-chip for testing purposes are different, allowing some refinements in the test procedures.

Our proposal performs the above-mentioned verification by using only the hardware and software resources of the μC, minimizing consequently the cost in hardware overhead and power consumption. This characteristic is one of the contributions of this paper, but it is also the main challenge. In addition, the ACT experimental evaluation is performed in an embedded system-based application board, which consists of a wireless sensor network (WSN) node with a multisensor interface capability. This constitutes another important contribution of the present work due to the fact that the performance of the ACT approach is evaluated in a real application context. The results show that the ACT concept can be successfully extended to the case under study.

The rest of this work is organized as follows: in Section 2, a brief description of the application platform and general test considerations are presented. In Section 3, the implementation of the ACT approach is explained. The experimental results are reported in Section 4. Finally, Section 5 concludes the paper.

2. System under Test

2.1. Application Board. As previously mentioned, the ACT experimental evaluation was performed in a real application board (see Figure 1(a)), which consists of a WSN node. Figure 1(b) shows its complete hardware block diagram. A MSP430 microcontroller (MSP430FG4619) and the set of RF transceiver and range extender (CC2500 and CC2591, resp.) are the essential components of the node. Additionally, the board is endowed with a multiple-sensor configurable interface: three channels for connecting digital sensors (DCH_X in Figure 1(b)) and three analog counterparts (ACH_X). Each channel is composed of a set of terminals, some of which have variable functionality according to the interface requirements of the respective sensor.

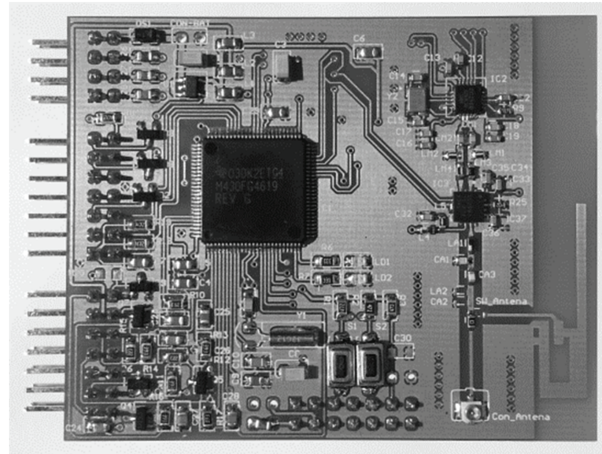
In particular, the analog channels must support the direct connection of a wide range of sensors with different analog interfaces to a fixed hardware structure. This implies that these channels should have the resources required to perform two main processes: the conditioning and the digitalization of the sensor signal. For doing these tasks, the node exploits the reconfiguration capability of the analog and mixed signal resources available in the μC. The implementation of this concept is illustrated in Figure 2.

As shown in the above-mentioned figure, the microcontroller resources assigned to the analog channels are: an embedded OA module (OAM), which is used in the conditioning signal stage, an ADC, responsible for performing the digitization process, and a digital-to-analog converter (DAC), employed when the configuration of the interface requires the generation of an offset or a reference voltage level. In addition, outside the μC boundaries, each analog channel (ACH_X) has a structure of discrete components, needed to form the circuit configurations used in the acquisition of sensor signals. These external components can be dynamically disconnected from the signal path (according to the requirements of the programmed interface) by means of the proper configuration of analog pins or through the analog switches arranged for that purpose.

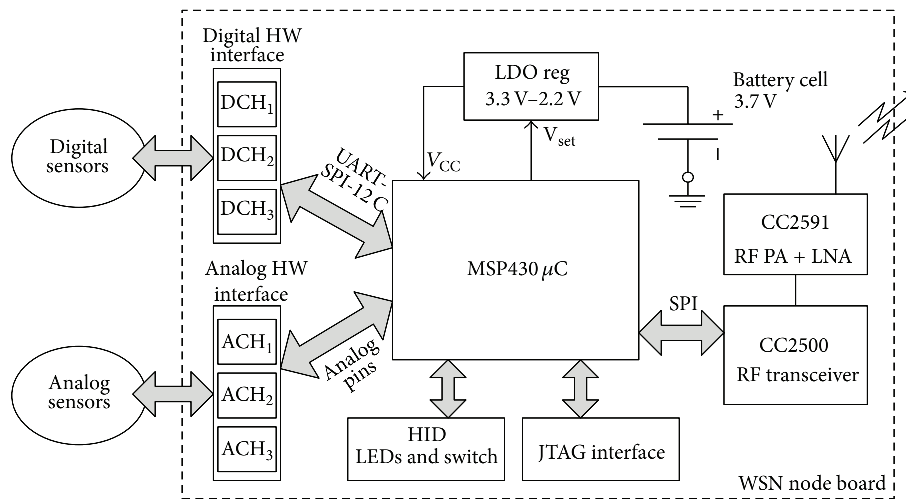
For the sake of clarity, Figure 3 presents examples of the interface configurations used for certain analog sensors. In these examples, it is possible to appreciate the changes in the OAM functionality. In Figure 3(a), the module is programmed as a unity-gain buffer for resistive type sensors. A programmable-gain noninverting amplifier is configured for output-voltage sensors (Figure 3(b)) in order to achieve the best input dynamic range of the ADC. Finally, the OA is used as a differential amplifier with external components (Figure 3(c)) for bridge-type sensors. Changes in the channel configuration can be done on field, during the network normal operation by the reception of the corresponding configuration packet.

2.2. OA Module Description. Three OAMs (OAM0, OAM1, and OAM2) are implemented in the MSP430xG461x devices. The functional diagram of one of these modules is depicted in Figure 4. As it is shown, an OA_X (where X is used to indicate which OA module is being discussed), several analog multiplexers, a resistor ladder, and other resources compose each OAM. The block configuration is register-based and is programmed by the user at runtime. Each OAM can be configured to work individually or in combination with other modules, by means of internal feedback paths or using external components.

All the multiplexers and switches driven by the signal *mode selection* establish different module configurations, called by the manufacturer as "Modes" (see Table 1). The input source for the module is selected by using *N-input selection* and *P-input selection* signals. The OAM output is configured



(a)



(b)

Figure 1: WSN node. (a) Board photograph. (b) Hardware block diagram.

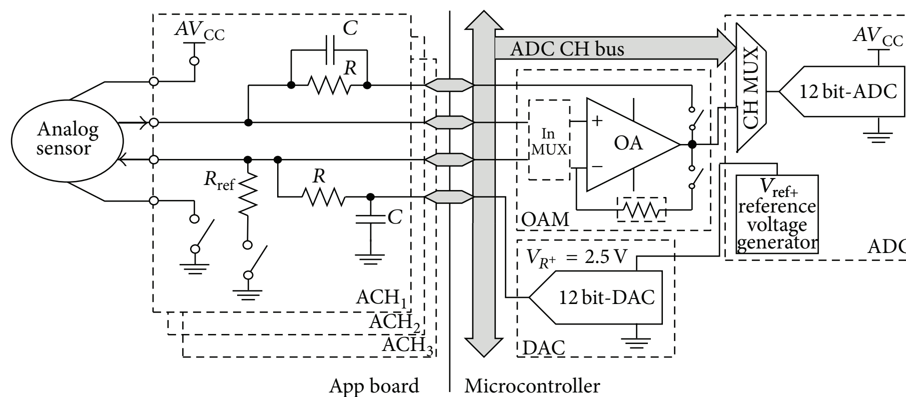


Figure 2: Analog sensor interface of the WSN node.

by two different signals. The signal *output-1 selection* allows the internal routing to some special inputs of the ADC, while the signal *output-2 selection* permits the connection of the OA output signal (*OAxOUT*) with dedicated analog output pins. The internal connection of two or more OAMs is possible due to the signals *OAxOUT, OAxTAP*, and *OAxR bottom*. The programmable resistor ladder provides the gain in amplifier modes, as well as the reference voltage level in comparator mode, by the use of the multiplexer driven by the signal *gain selection*.

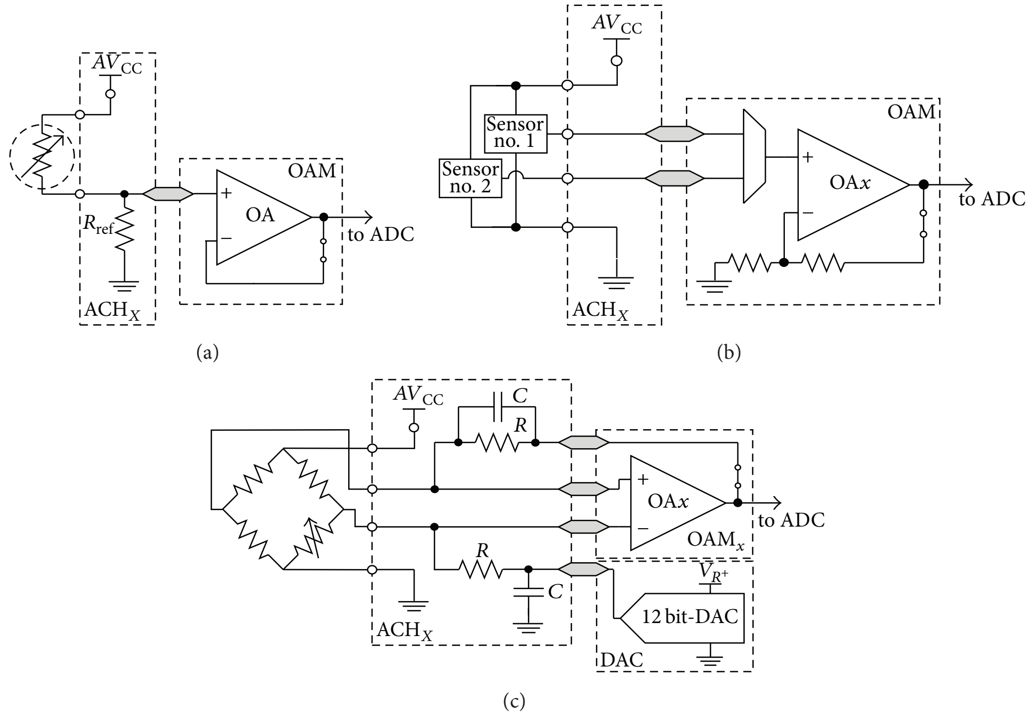


Figure 3: Examples of analog sensor interface. (a) Resistive type. (b) Output voltage. (c) Bridge type.

It is possible to change the slew rate of the OA by using the *slew rate selection* signals. These signals set three active modes: slow, medium, and fast. Additionally, unlike the OAM used in [14], the OA input dynamic range is also configurable here and the rail-to-rail input mode can be disabled, causing a significant reduction in OA quiescent current. The manufacturer provides further details of the module in [17].

2.3. Test Considerations. The μC adopted in the node implementation is based on a 16-bit RISC CPU and includes several digital, analog, and mixed-signal modules on-chip. The complete block diagram of the device, obtained from its datasheet [18], is depicted in Figure 5. This figure shows the OAMs identified as circuits under test (CUT) and highlighted the resources used by ACT.

The OAM addressed in this work is different from the one used in [14]. This can be clearly appreciated by simply comparing their full schematic diagrams, reported in [17, 19] by the manufacturer. The internal feedback structure, the circuitry associated with OA output handling, and the module input options are the most noticeable differences. Additionally, the configuration registers of both modules are not equal. Another factor that directly affects test procedures is the largest number of possible interconnection paths between OAMs, mainly due to the increase of the available circuits in this device.

In addition, it should be noted that not all possible configurations of *N-input selection* and *P-input selection* signals (See Figure 4) can be evaluated in the test procedures because the external OA analog input pins are reserved for application purposes in normal operation. Consequently, all the test procedures are performed using exclusively internal feedback paths, with the only exception of the procedure in mode 0, which requires an external feedback path.

Table 1: OAM modes.

Mode selection signal value	OAM mode
0	General-purpose OA
1	Unity gain buffer
2	Reserved
3	Comparator
4	Noninverting PGA[a]
5	Reserved
6	Inverting PGA
7	Differential amplifier

[a]PGA: programmable gain amplifier.

As can be seen in the next sections, our ACT determines the correctness of a number of programmed OAM configurations by measuring their gains. The on-chip digital-to-analog converter (DAC12 in Figure 5) is used as test stimulus generator. The internal analog paths connect the generator with the required destinations. Taking advantage of the availability of the DAC in this new platform, we use two different voltage levels for each test (V_{IN1} and V_{IN2}) and calculate the gain in differential form in order to cancel the effect of the OA offset level:

$$G = \frac{V_{OUT2} - V_{OUT1}}{V_{IN2} - V_{IN1}}. \quad (1)$$

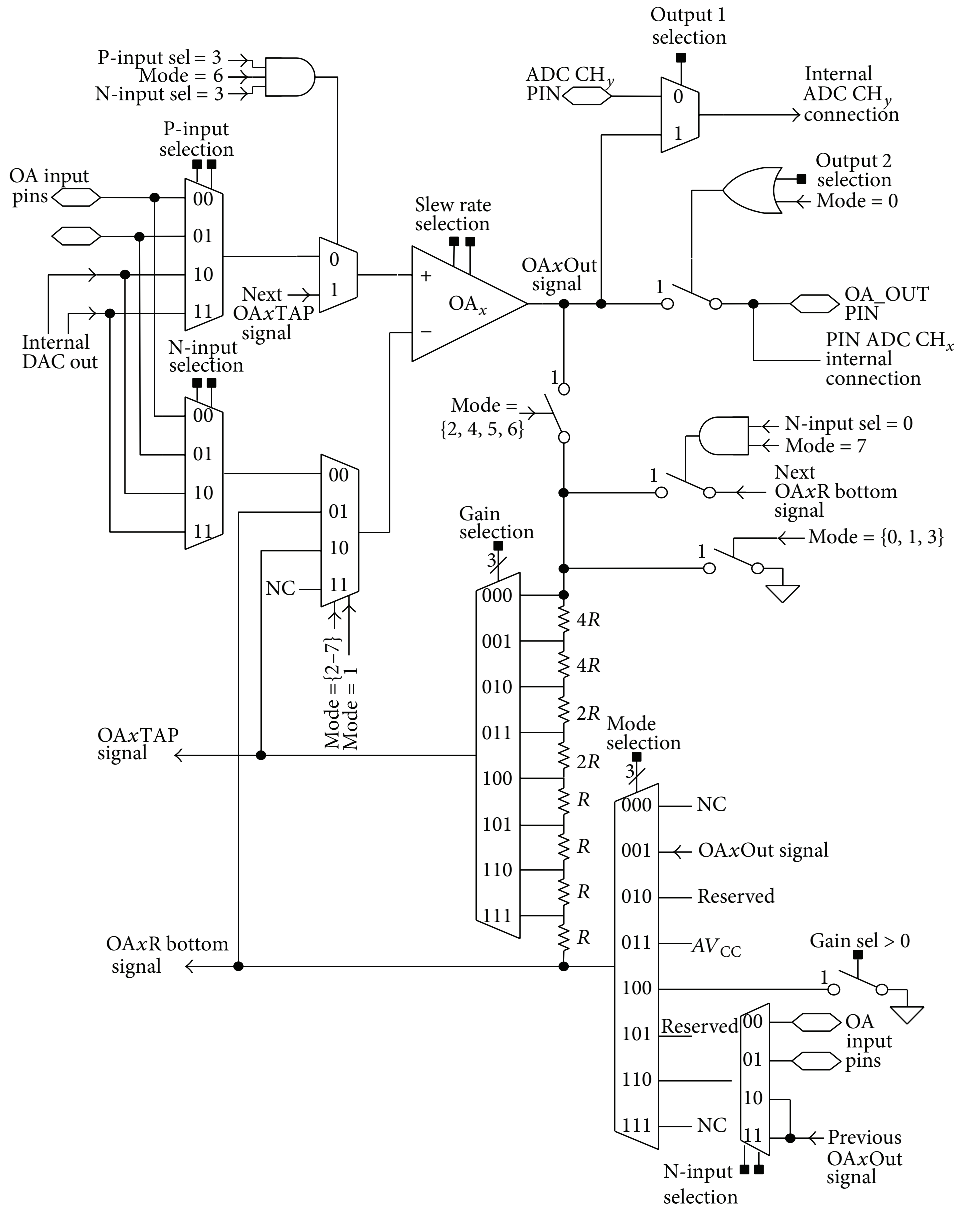


Figure 4: Schematic diagram of an OA module.

For this case study, all the measurements in test mode (excepting the slew rate) are performed using the internal ADC. As shown in Figure 5, the module is a 12-bit SAR core converter with 12 input channels (CH), sample select control, and on-chip reference voltage generator. The analog supply voltage of the device (AV_{CC}) is set as the reference voltage for the ADC in order to be able to perform conversions in the entire OA operating range.

The ADC inaccuracies (including offset, gain, and nonlinearity errors) introduce errors in the measurements performed by the routine. The total unadjusted error determines the overall deviation in the digital code delivered by the ADC from an ideal conversion. The datasheet reports a typical value of ±2 LSB for this parameter with a maximum of ±5 LSB, which means a maximum deviation of ±3.052 mV for our test conditions. This value is considered here as the limiting error of the voltage measurements, neglecting the noise. For declaring a given test parameter as faulty, it is necessary to take into account both the device tolerances related to the fabrication process and the limiting error. Detailed information on the calculations required for determining the acceptance ranges for a similar case can be found in [14].

3. Analog Configurability Test Scheme

The ACT approach is based on an embedded test routine that mainly performs four different tasks. The first one checks the voltage relations of the resistor ladder by acquiring the voltage level at its internal connection points. The second task tests the configurability of the available modes by programming

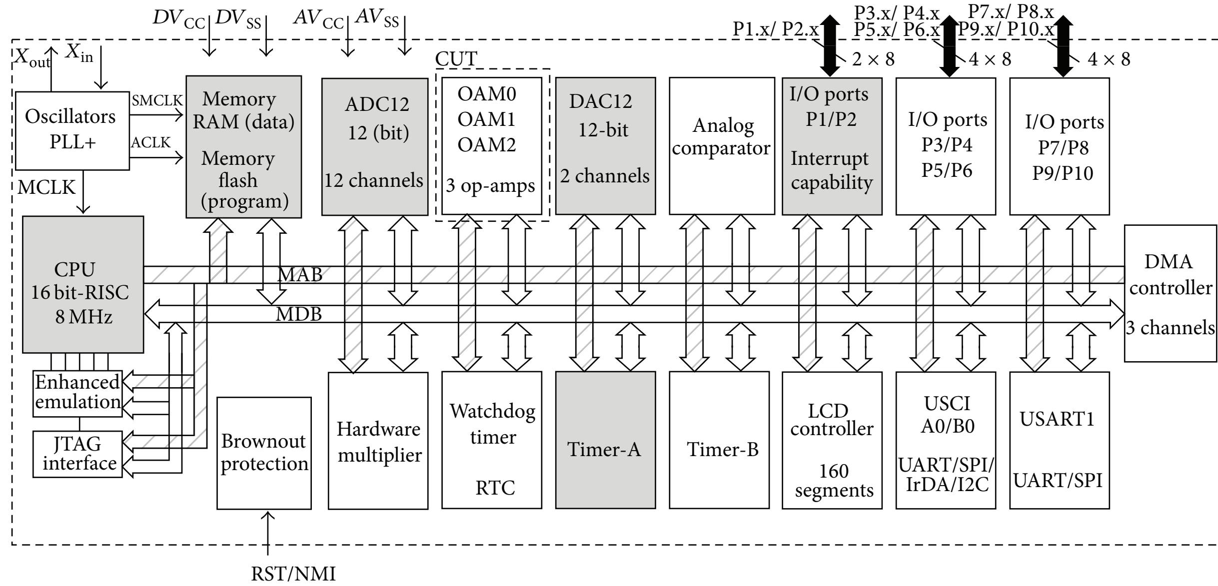


Figure 5: Block diagram of the MSP430FG4619 used as a case study.

Table 2: OAM valid configurations versus used by ACT.

OAM mode	OAM valid configurations	ACT task	Configurations used by ACT
Mode 0	12	Mode 0 configurability test	1
Mode 1	24	Mode 1 configurability test	1
Mode 3	192	Mode 3 configurability test	2
		Resistor ladder test	8
		Slew rate test	6
Mode 4	192	Mode 4 configurability test	1
Mode 6	384	Mode 6 configurability test	2
		Input rail-to-rail mode test	8
Mode 7	192	Mode 7 configurability test	1
Totals	**996**		**30**

selected gains. Then, the configurability of the slew rate of each OA is verified in the third task, by measuring the time taken by the OA output to achieve a given value. Finally, the last task determines if the rail-to-rail input mode can be enabled and disabled by the user.

In order to test the correct block programmability, it is necessary to exercise all the possible states of the multiplexers and switches, employing all the configuration signals combinations. In addition, all possible signal paths in the module should be used. Each OAM has seven groups of configuration signals: *gain selection* (3 bits), *output selection* (2 bits), *mode selection* (3 bits), *slew rate selection* (2 bits), *input rail-to-rail mode selection* (1bit), *P-input selection* (2 bits), and *N-input selection* (2 bits). If the two last groups of signals are not taken into account because, as mentioned above, we reserve the OA analog input pins for application purposes, the remaining signals produce 256 possible configurations for each value of *mode selection* signal (an OAM mode).

However, not all the combinations are valid for all the modes due to the fact that there are some programmed configurations that have no effect in the module operation. For example, if the module is programmed in mode 0 (general-purpose OA), the internal feedback loop is automatically disconnected and, consequently, any change in the configuration signal *gain selection* does not produce changes in the signal path. In this way, the number of valid combinations for mode 0 is reduced to 12 active configurations (2 valid combinations for *output 1 selection*, 2 combinations for *input rail-to-rail mode selection*, and 3 slewrate active modes). Table 2 summarizes the number of valid combinations for each mode in the column labeled as “OAM valid configurations,” based on the reduced structural information provided by the vendor in [17].

As can be inferred from this analysis, an exhaustive exercise of all the valid OAM configurations would be extremely costly in both time and power consumption. However, the

Table 3: Test conditions and expected values for the resistor array.

Test condition	Configuration	Ideal value for V_{OAxTAP} ($\mathrm{AV_{CC}}$ units)
1	Gain selection = 1	0.2500
2	Gain selection = 2	0.5000
3	Gain selection = 3	0.6250
4	Gain selection = 4	0.7500
5	Gain selection = 5	0.8125
6	Gain selection = 6	0.8750
7	Gain selection = 7	0.9375

proper selection of test configurations allows exercising all the possible states of the multiplexers and switches while covering all the signal paths for each module. The next subsections provide further details about the test procedures and the OA configurations. In this sense, Table 2 also reports the number of combinations used by the ACT for each task in the test routine.

3.1. Resistor Ladder Test. Our test approach seeks to establish whether all the internal connection points of the OAM resistor ladder are available for the application. For doing this task, we set the OAM in mode 3 (comparator). In this mode, the multiplexer driven by *gain selection* establishes a programmable voltage reference at the *OAxTAP signal* (see Figure 4). The resistor ladder is divided into two: R_{top} (with its top end connected to analog ground) and R_{bottom} (with its bottom end connected to the analog power supply $\mathrm{AV_{CC}}$). In this way, the V_{OAxTAP} (voltage at *OAxTAP signal*) value is

$$V_{\mathrm{OAxTAP}} = \frac{R_{\mathrm{top}}}{R_{\mathrm{bottom}}+R_{\mathrm{top}}} \cdot \mathrm{AV_{CC}}. \quad (2)$$

Table 3 reports the expected values for V_{OAxTAP} for each test condition used by ACT.

Because it is not possible to measure directly V_{OAxTAP} through an ADC input channel, we propose the scheme depicted in Figure 6. This figure shows the OAMs setup configured by the test routine, valid for the three modules. The signal *OAxTAP* is cascaded with the next OAM configured as a unity gain buffer in mode 6. In this way, the ADC acquires (in CH12, CH13, and CH14 for OAM0, OAM1, and OAM2 resp.) the programmable V_{OAxTAP} value of the CUT. It should be mentioned that, prior to this test procedure, all OAMs are exercised in mode 6 as unity gain buffer in order to check their right operation.

From the measurement of these voltages, the test routine determines if all the relations of R_{top} and R_{bottom} can be programmed and checks if their values are within the limits specified by the user. As the resistance ratios establish the gain for the other module configurations, the routine indirectly tests the correctness of these gain values. Consequently, it would be not necessary to test all the available gain configurations in the ACT procedures.

3.2. Mode Configurability Test. To confirm the correct configurability of each OAM mode, ACT determines the gain of the block in different configurations (to be presented in the next subsection). If this parameter is within the limits allowed by the applications needs, then it is accepted that the tested mode has been properly programmed.

3.2.1. Test of Modes 0 and 1. In both modes, the OAMs are configured as unity gain buffers. Mode 0 is designed for using the module with external components and all the internal feedback paths are isolated from the OAs. Consequently, for configuring the OA as unity gain buffer, we use the OA pins to connect the feedback loop. Figure 7 shows the scheme adopted. The feedback path is a wired connection taking advantage of the existing components on the application circuit board. However, if the configuration of a specific application does not include a resistor feedback path, the use of external analog multiplexers (to switch between test and normal operation mode) is required. Otherwise, the test procedure for mode 0 (like any other ACT procedure) can be overridden according to the test requirements of the application. In mode 1, the OA is configured as unity gain buffer using a dedicated internal feedback path.

The test procedure is the same for both modes. The OA output is connected to the ADC input channel assigned to the OAxOut pin (OA0, OA1, and OA2 with CH0, CH1, and CH2, resp.). The ADC also acquires the OAM input signal (test stimulus) from the DAC1 output through the CH7. With these values, the on-chip processor computes the gain.

3.2.2. Test of Mode 3:Comparator. For testing this mode, we set a fixed voltage level at the noninverter input of the OAs (V_+) by using the DAC1 internal connection and program the inverter input with voltages obtained from the resistor ladder. By commuting the ladder between voltages higher and lower than V_+, it is possible to verify if the comparator output transitions are between the values reported by the vendor in [18]. The ADC acquires the OA output values using the internal routing to the ADC CH12, CH13, and CH14 for OAM0, OAM1, and OAM2, respectively.

3.2.3. Test of Mode 4:Noninverting PGA. In order to test the mode 4 programmability, we set the gain of each OAM as 2. As the right operation of the resistor ladder is previously tested, only one value for the gain is used in the test procedure. As shown in Figure 8, DAC1 is used for exciting the OAMs with DC voltage levels. The OAMs input stimulus is registered through the ADC CH7, while the OAs outputs are measured as in the test of mode 3.

3.2.4. Test of Mode 6:Inverting PGA. When an OAM is configured in mode 6 (programmable-gain inverting amplifier), the use of a positive DC voltage level as test stimulus is not useful because the μC employs a single supply. Consequently, a negative output swing is not possible. However, for testing mode 6, it is possible to configure the OAM as inverter amplifier but connect internally its input to ground by means of the proper configuration of the OA input pin. This can be observed in Figure 9 for the module labeled as "CUT I."

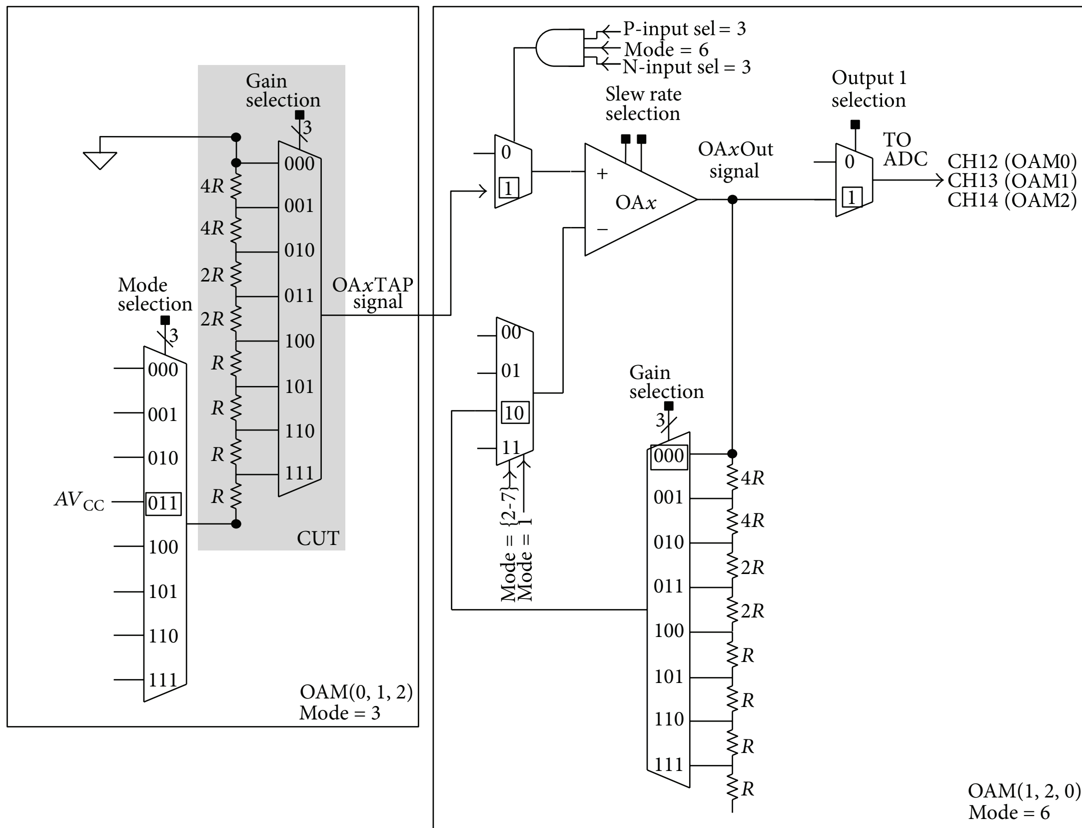


Figure 6: Setup of OA modules for testing the resistor arrays.

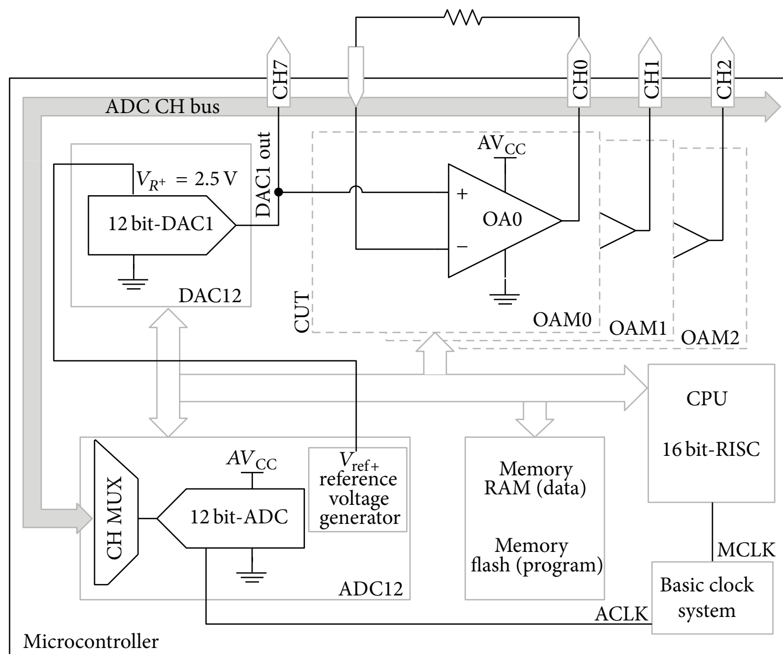


Figure 7: Arrangement for testing mode 0.

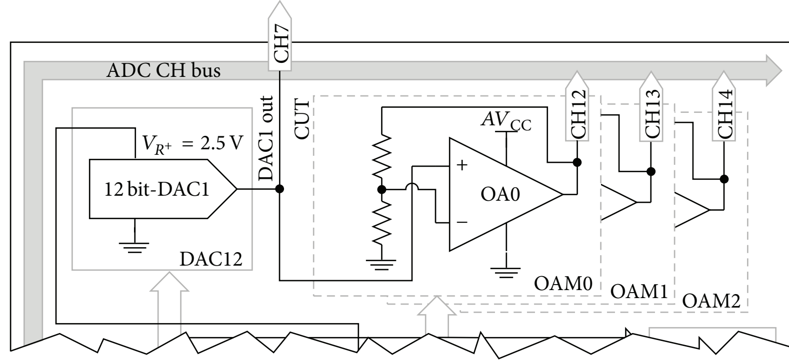


FIGURE 8: Arrangement for testing mode 4.

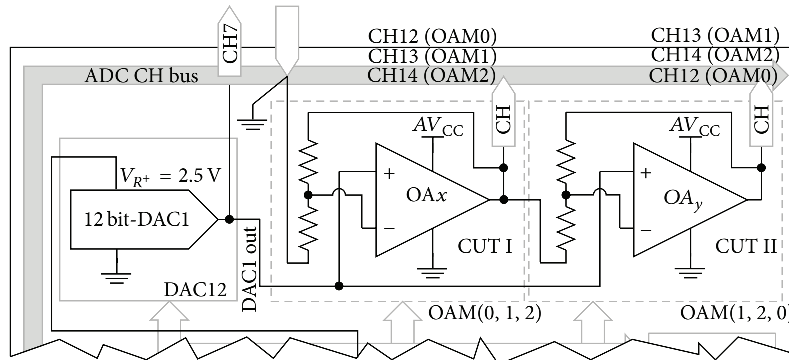


FIGURE 9: Arrangement for testing mode 6.

Under the above-mentioned condition, if the OA noninverter input is connected to a DC voltage from the DAC 1, then the system behaves like a noninverter amplifier with the CUT programmed in mode 6. In this way, it is possible to test individually the mode configurability of each OAM. As in the previous case, the gain of the amplifier is set as 2 and the ADC acquires the input/output levels of each module by means of the channels reported in Figure 9.

Another feature that characterizes an OAM in mode 6 is that it can be cascaded with the previous OAM output. This situation can be observed for the module labeled as "CUT II" in Figure 9. With the aim of verifying these interconnection paths, the test routine also configures the pair of OAMs as shown in the above-mentioned figure and registers the voltage level at the positive input of both OAs ($V_{\text{DAC1_Out}}$) and the output of the cascade connection (output of CUT II), named as $V\text{out}_{\text{OAy}}$. In this way, the routine determines whether the cascade connection can be programmed, by computing the gain achieved by the array. This process is repeated three times, one for each possible combination (OAM0-OAM1, OAM1-OAM2, and OAM2-OAM0).

Under these conditions, the gain of the cascaded amplifiers is

$$G_{\text{cascade}} = \frac{V\text{out}_{\text{OAy}}}{V_{\text{DAC1_Out}}} = G_{\text{OAx}} \cdot G_{\text{OAy}} + 1 - G_{\text{OAy}}. \quad (3)$$

In (3), G_{OAx} and G_{OAy} are the programmed gain values for OAM_X and OAM_Y, respectively. If this gain is not achieved for a given cascade connection, the interconnection path is declared faulty since each module has been previously tested individually.

3.2.5. Test of Mode 7:Differential Amplifier. The μC adopted as a case study supports a three-OA differential-amplifier configuration. The manufacturer reports in [17] the OAMs setup for this configuration, depicted in Figure 10. The output voltage is calculated as

$$V_{\text{diff}} = \frac{(V_2 - V_1) \cdot R_2}{R_1}. \quad (4)$$

For testing mode 7 configurability, we inject a DC stimulus to the input labeled as V_2 by means of the DAC1, and V_1 is connected internally to power ground. Then, we evaluate through the ADC the OA_Z output (V_{diff}) and establish the gain value V_{diff}/V_2. This process is repeated three times, changing the OAM programmed on mode 7 (CUT).

3.3. OA Input Swing Testing. As mentioned in Section 3, the OA input signal swing is software selectable by using the *OARRIP* configuration signal. The user can select between two possibilities: rail-to-rail input range (−0,1 V to AV_{CC} + 0,1 V) or limited input range (−0,1 V to $\text{AV}_{\text{CC}} - 1,2$ V). All the above-mentioned test procedures were performed with the OAMs configured in rail-to-rail mode. However, if the user limits the amplifier input range, the gain of the block should

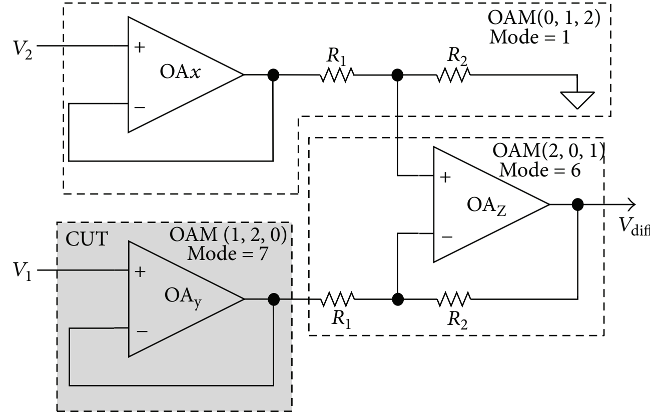


Figure 10: Three-OA differential amplifier configuration.

be less than the nominal value for input voltage levels near AV_{CC}.

In order to test the OA input swing programmability, the OAMs configuration depicted in Figure 6 is used. The test routine limits the OA_X input range by setting the *OARRIP* signal and the resistor ladder is used to set the stimulus levels near AV_{CC} due to the fact that the DAC output voltage is limited up to 2.5 V. The new OA_X output measurements are performed as explained in Section 3.1. The block gain is computed by means of these measurements and the registered ones during the resistor ladder test procedures. If the gain of the OA_X module is less than the unit for the three last test conditions reported in Table 3, then the routine determines that the rail-to-rail input mode was successfully disabled.

3.4. Slew Rate Testing. Each OA has three active modes: slow (0.3 V/μs), medium (0.8 V/μs), and fast (1.2 V/μs). These slew rate (SR) values are achieved by changing the *slew rate selection* configuration signals, shown in Figure 4. In order to test the right configuration of this parameter, ACT uses the internal timer module to measure the time that takes the OA output for making a transition from a low voltage level (V_{OL}) to a high one (V_{OH}), for the three active modes.

Figure 11 depicts the scheme adopted for this part of the test routine. As observed, the OAM is configured as comparator. A reference voltage from the resistor ladder and the DAC1 output are connected to the OAx inputs. The output of each OA under test is connected to a general-purpose digital-input pin with interrupt capability using an external wired connection (exclusively for testing purposes). These pins generate an interrupt when there is a low-to-high transition at the *OAxOut* signal. The routine uses this interrupt resource and the Timer-A module, configured at the lowest available period (125 ns), to accomplish the time measurements.

The test procedure is represented in Figure 12(a). While the OA noninverting input voltage V_{in+} has a constant level from the DAC1 module, V_{in-} is switched from a voltage level higher than V_{in+} to a lower one by changing the configuration of the resistors ladder. This produces a transition at the OA output (called V_{OAout}) from V_{OL} to V_{OH}. At the same time, Timer-A is reset and starts a count. When this signal reaches the threshold voltage of the digital input pin (V_{IT+}), the pin generates an interruption and the timer is stopped.

According to this figure, the SR can be estimated as

$$SR = \frac{V_{IT+}}{t_{sr\,\mu C}}, \tag{5}$$

where

$$t_{sr\,\mu C} = t_{TA\mu C} - t_d - t_{int}, \tag{6}$$

$$t_{TA\mu C} = \frac{1}{f_{clkTA}} \cdot \text{Count}_{TA}. \tag{7}$$

In (6), $t_{TA\mu C}$ is the time measured with Timer-A and t_d represents the dead time of the OA, defined in this work as the time required by the OA to reach the 5% of its final value when a step stimulus is applied. On the other hand, t_{int} is the interruption processing time and is defined here as follows: the time between the comparator output voltage reaches V_{IT+} and the test routine stops the timer. In (7), Count_{TA} is the count reached by the Timer-A register and f_{clkTA} is the work frequency of the timer.

The parameters t_d, t_{int}, and V_{IT+} used by the test routine in the SR estimation are experimentally determined. For doing this task, the routine generates an auxiliary signal ($V_{aux\mu C}$ in Figure 12) in a digital-output pin that registers the timer events (when it starts and stops the count). This signal allows the measurements of times and voltage shown in Figure 12(b). The figure presents the results of three measurements on a single OAM, one for each possible SR configuration. However, the measurements have been time-shifted to match the low-to-high transition of the signal $V_{aux\mu C}$ (stop count timer event). In this way, the intersection point of the three V_{OAxOut} signals is used as a reference in the measurement of t_{int} and V_{IT+}, because these parameters are independent of the SR configuration. Additionally, it is possible to clearly determine the different values of t_d.

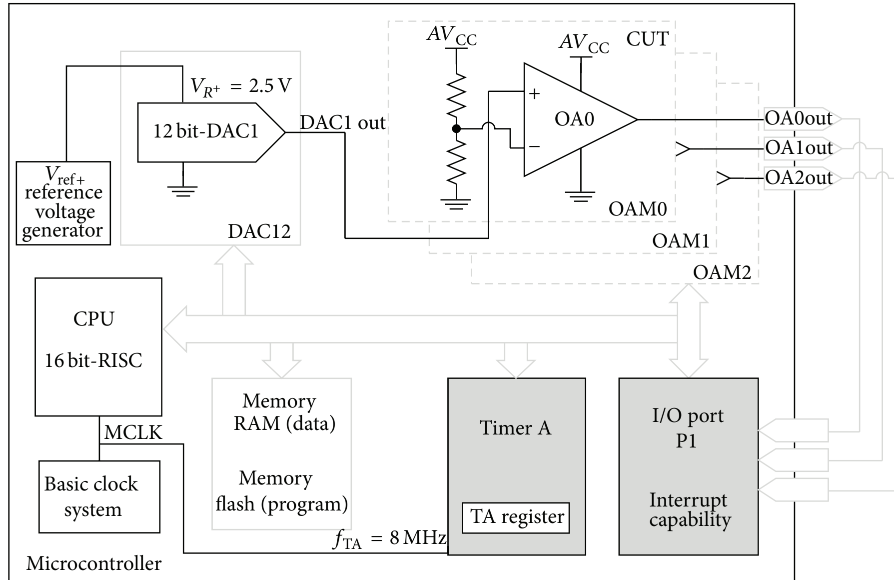


Figure 11: Arrangement for testing slew rate.

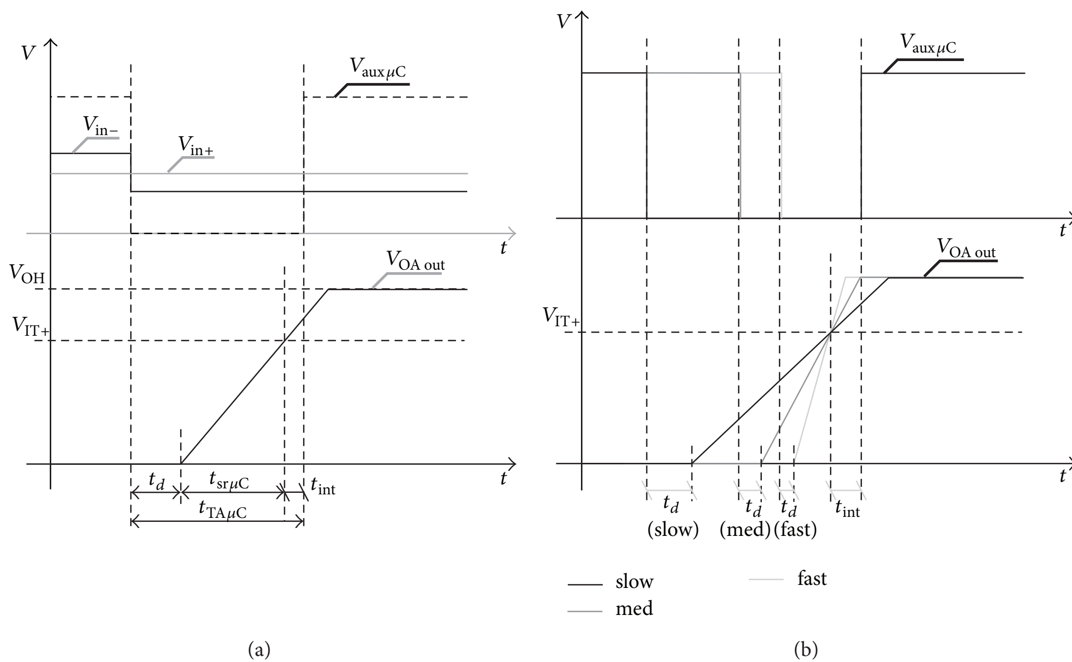


Figure 12: (a) Slewrate test timing diagram. (b) Experimental measurement of t_d, t_{int}, and V_{IT+}.

4. Experimental Test Results

The embedded test routine is written in C language as a library using IAR Embedded Workbench for TI MSP430 C/C++ compiler and amounts to about 3 Kbyte of program memory in the μC. For the device used in this application (MSP430FG4619), the total routine execution time is 53.5 ms with a CPU clock (main clock, MCLK) of 1 MHz. The measurement repeatability at free air temperature is evaluated in order to assess the test precision. For doing this task, the test procedure is repeated 100 times in each test condition.

Table 4 summarizes the test results for the resistor ladder. It presents the measured values of V_{OAxTAP} in each test condition detailed in Table 3, for all the OAMs available in the device. The mean values shown in the table are a measure of central tendency, while the maximum (Max) and the minimum (Min) values are a measure of dispersion. All the values depicted in the table are expressed in AV_{CC} units. As can be seen from the data, all measurements present a very low dispersion around the mean value and are very similar for all the OAMs. The maximum deviation is 0.177% (related to the mean value) for the minimum value of test condition 6

Table 4: Resistor ladder test experimental results.

Parameter	Test condition	Min	Mean	Max
Voltage level available at the resistor ladder OA0 V_{OA0TAP} (AV_{CC} units)	1	0.2505	0.2506	0.2510
	2	0.4999	0.5002	0.5006
	3	0.6247	0.6250	0.6256
	4	0.7497	0.7500	0.7507
	5	0.8122	0.8126	0.8132
	6	0.8742	0.8747	0.8750
	7	0.9368	0.9371	0.9382
Voltage level available at the resistor ladder OA1 V_{OA1TAP} (AV_{CC} units)	1	0.2505	0.2508	0.2510
	2	0.4999	0.5003	0.5006
	3	0.6247	0.6249	0.6256
	4	0.7492	0.7497	0.7502
	5	0.8117	0.8121	0.8122
	6	0.8730	0.8746	0.8750
	7	0.9355	0.9368	0.9372
Voltage level available at the resistor ladder OA2 V_{OA2TAP} (AV_{CC} units)	1	0.2498	0.2502	0.2505
	2	0.4996	0.5000	0.5001
	3	0.6247	0.6248	0.6249
	4	0.7497	0.7499	0.7507
	5	0.8117	0.8122	0.8127
	6	0.8730	0.8744	0.8747
	7	0.9355	0.9366	0.9372

in OAM1. By another way, the mean values are very close to the nominal values reported in Table 3. The highest deviation from nominal values is 0.323% observed for test condition 1 in OAM1. This value can be taken as an indicator of the high accuracy achieved by ACT.

The experimental results for modes 0, 1, 4, 6, and 7 are reported in Table 5. The column labeled as "Parameter" shows the specific gains evaluated by the test routine for each OAM mode. The column labeled as "Test setup" shows the expected value for these parameters and gives the value of the *gain selection* signal (see Figure 4). The columns "Min," "Mean," and "Max" depict the lowest, mean, and highest values of the parameters for the 100 repeated measurements. As in the case of the resistor ladder test, the table shows that the measurement repeatability is very good for all the modes tested. The highest observed deviation is 1.02% in mode 0. By another way, the mean values are very close to the expected for each programmed configuration, with a maximum deviation of 0.38% in mode 7.

The test of mode 3 shows that all the OAMs, configured as comparators, give output excursions between 3.3 mV and values near AV_{CC}, for the 100 repeated test executions. This range agrees with the data reported by the vendor in the datasheet [18]. On the other hand, the test results related to the OA-input swing configurability show that the module gain (with the range limited) is always less than the unit for the three last test conditions reported in Table 3. These values can only be achieved if the rail-to-rail input mode is successfully disabled.

Table 6 depicts the experimental results related to the slewrate test procedures, obtained in 100 test executions. The table shows that the slewrate measurements present virtually no dispersion, with the exception of the values for the OA0 and OA2 in "medium" configuration, registering a maximum variation of 9.53% with respect to the main value. As mentioned in Section 3.4, the Timer-A is working at the highest allowed frequency (8 MHz), producing quantization errors in the slew rate measurements of 1.532%, 4.226%, and 7.154% for the slow, medium, and fast configurations, respectively.

The quantization error values and the experimental data (reported in Table 6) confirm that ACT distinguishes changes in the slewrate and consequently is able to test its configurability because the errors are significantly smaller than the percentages of variations in the SR produced by a change of configuration. With the aim of comparison, Table 6 also includes the slewrate typical values reported by the vendor. For all OAs, the mean values are near to the typical ones, suggesting that the measurement is a good estimator of the parameter.

Table 7 shows the auxiliary measurements of times used in the slewrate estimation: interrupt processing time (t_{int}) and dead time (t_d). The values in the table are the result of the measurements performed experimentally in laboratory. As

Table 5: Modes test experimental results.

Test mode	Parameter	Test setup	Min	Mean	Max
Mode 0	Unity gain OAM0		0.9939	1.0013	1.0075
	Unity gain OAM1		0.9917	1.0010	1.0083
	Unity gain OAM2		0.9947	1.0011	1.0114
Mode 1	Unity gain OAM0		0.9969	1.0026	1.0091
	Unity gain OAM1		0.9954	1.0025	1.0098
	Unity gain OAM2		0.9916	0.9979	1.0045
Mode 4	Gain OAM0	Programmed gain = +2 Gain selection = 2	1.9879	2.0036	2.0167
	Gain OAM1		1.9924	2.0041	2.0182
	Gain OAM2		1.9894	2.0025	2.0152
Mode 6	Gain OAM0	Programmed gain = +2 Gain selection = 2	1.9894	2.0020	2.0198
	Gain OAM1		1.9894	2.0029	2.0167
	Gain OAM2		1.9939	2.0035	2.0167
	Gain OAM2-OAM0 in cascade	Programmed gain = 0.665 Gain selection OAM2 = 1 Gain selection OAM0 = 2	0.6626	0.6672	0.6727
	Gain OAM0-OAM1 in cascade	Programmed gain = 0.665 Gain selection OAM0 = 1 Gain selection OAM1 = 2	0.6619	0.6668	0.6717
	Gain OAM1-OAM2 in cascade	Programmed gain = 0.665 Gain selection OAM1 = 1 Gain selection OAM2 = 2	0.6611	0.6671	0.6709
Mode 7	Gain of arrangement OAM0-OAM1-OAM2	Programmed gain = 1.666 CUT = OAM1	1.6591	1.6724	1.6823
	Gain of arrangement OAM1-OAM2-OAM0	Programmed gain = 1.666 CUT = OAM2	1.6591	1.6721	1.6818
	Gain of arrangement OAM2-OAM0-OAM1	Programmed gain = 1.666 CUT = OAM0	1.6601	1.6730	1.6859

Table 6: Slew-rate test experimental results.

Parameter	Programmed slew rate	Typical	Min	Mean	Max
Slew rate OA0 (V/μs)	Slow	0.300	0.255	0.255	0.255
	Medium	0.800	0.702	0.743	0.770
	Fast	1.200	1.226	1.226	1.226
Slew rate OA1 (V/μs)	Slow	0.300	0.264	0.264	0.264
	Medium	0.800	0.770	0.770	0.770
	Fast	1.200	1.226	1.226	1.226
Slew rate OA2 (V/μs)	Slow	0.300	0.240	0.240	0.240
	Medium	0.800	0.702	0.703	0.770
	Fast	1.200	1.226	1.226	1.226

Table 7: Slew rate test auxiliary measurements.

Programmed slew rate	Interrupt processing time t_{int} (μs)	Dead time t_d (μs)
Slow	2.3	7.92
Medium	2.3	2.62
Fast	2.3	1.58

can be seen from the table, t_{int} value is independent of the OAM configuration because it only depends on the frequency of the CPU clock (MCLK).

5. Conclusions

In this paper, we address the application of the ACT approach to an EACC composed of operational amplifiers and interconnection resources of a modern μC. The proposed scheme allows establishing the correct configurability of the CUT and checks the proper behavior of the resistor arrays. The test procedures were successfully adapted to the requirements of the addressed EACC. The negligible hardware overhead of the approach allows using it as a low-cost self-test procedure for maintenance purposes in applications that require minimizing power and cost. The test strategy is experimentally evaluated in a WSN node with multisensor interface capability in order to demonstrate the ACT approach applicability in the context of a real application. The experimental results show very good repeatability, with very low errors. These results allow concluding that the approach proposed here is useful for testing the functionality of the CUT using a simple and very low-cost strategy.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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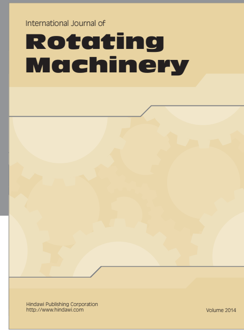
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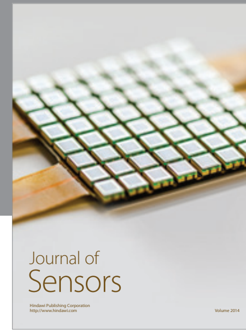
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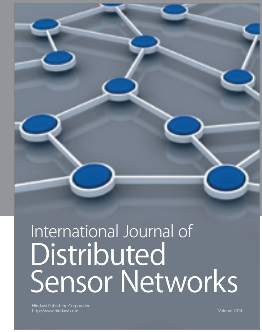
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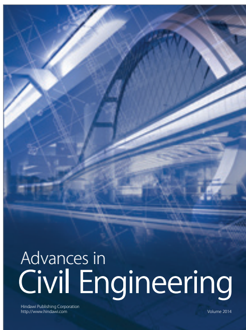
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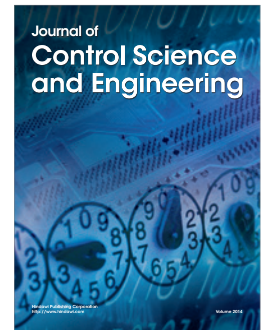
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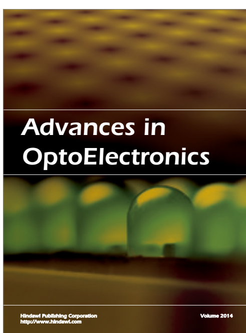
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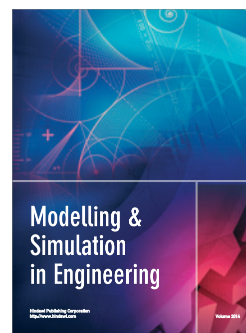
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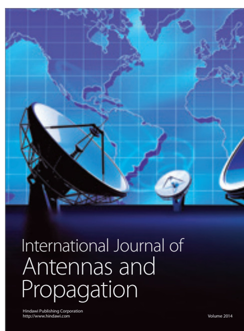
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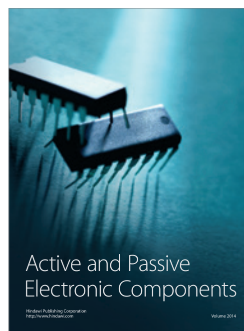
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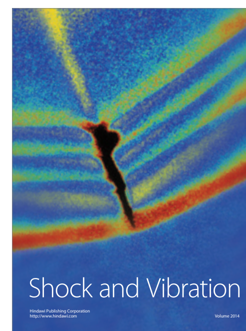
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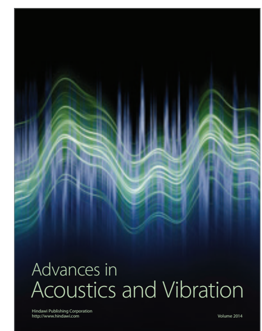
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